TEXAS INSTRUMENTS

TMS34010 Programmer's Reference

Memory Map

Address	15 … 0	
>FFFF FFF0 – >FFFF FC00	64 words	Interrupt vectors
>FFFF FBF0 – >FFFF E000	512 words	Reserved
>FFFF DFF0 – >C000 2000	2^{26} - 1024 words	General use
>C000 1FF0 – >C000 0200	512 words	Reserved
>C000 01F0 – >C000 0000	32 words	I/O registers
>BFFF FFF0 – >0000 0000	3×2^{26} words	General use

Status Register

31	30	29	28	27–26	25	24–22	21	20–12	11	10–6	5	4–0
N	C	Z	V	res	PBX	res	IE	reserved	FE1	FS1	FE0	FS0

N	Sign bit (or X=0)	**IE**	Interrupt enable
C	Carry bit (or Y<0)	**FE1**	Field extension bit 1
Z	Zero bit (or Y=0)	**FS1**	Field size bit 1
V	Overflow bit (or X<0)	**FE0**	Field extension bit 0
PBX	PixBlt executing bit	**FS0**	Field size bit 0

Register File B

Register	31(MSB) … 0(LSB)	Description
B0	SADDR	Source Address
B1	SPTCH	Source Pitch
B2	DADDR	Destination Address
B3	DPTCH	Destination Pitch
B4	OFFSET	Offset
B5	WSTART	Window Start
B6	WEND	Window End
B7	DYDX	Delta Y/Delta X
B8	COLOR0	Color 0
B9	COLOR1	Color 1
B10	Temporary Register	Used as temporary storage for PIXBLTs and FILLS
B11	Temporary Register	
B12	Temporary Register	
B13	Temporary Register	
B14	Temporary Register	
SP	Stack Pointer	

I/O Registers

Address	Register (15 … 0)	Description
>C000 01F0	REFCNT	DRAM refresh count
>C000 01E0	DPYADR	Display address
>C000 01D0	VCOUNT	Vertical count
>C000 01C0	HCOUNT	Horizontal count
>C000 01B0	DPYTAP	Display tap point
>C000 01A0 – >C000 0170	Reserved	
>C000 0160	PMASK	Plane mask
>C000 0150	PSIZE	Pixel size
>C000 0140	CONVDP	Conversion (dest. pitch)
>C000 0130	CONVSP	Conversion (source pitch)
>C000 0120	INTPEND	Interrupt pending
>C000 0110	INTENB	Interrupt enable
>C000 0100	HSTCTLH	Host control, 8 MSBs
>C000 00F0	HSTCTLL	Host control, 8 LSBs
>C000 00D0	HSTADRH	Host address, 16 MSBs
>C000 00E0	HSTADRL	Host address, 16 LSBs
>C000 00C0	HSTDATA	Host data
>C000 00B0	CONTROL	I/O control
>C000 00A0	DPYINT	Display interrupt
>C000 0090	DPYSTRT	Display start
>C000 0080	DPYCTL	Display control
>C000 0070	VTOTAL	Vertical total
>C000 0060	VSBLNK	Vertical start blank
>C000 0050	VEBLNK	Vertical end blank
>C000 0040	VESYNC	Vertical end sync
>C000 0030	HTOTAL	Horizontal total
>C000 0020	HSBLNK	Horizontal start blank
>C000 0010	HEBLNK	Horizontal end blank
>C000 0000	HESYNC	Horizontal end sync

Vector Address Map

Trap Number	Address	32 … 0	
0	>FFFF FFE0	[illegible]	Reset
1	>FFFF FFC0	[illegible]	External interrupt 1
2	>FFFF FFA0	INT2	External interrupt 2
3	>FFFF FF80	Traps 3–7	
4	>FFFF FF60		
5	>FFFF FF40		
6	>FFFF FF20		
7	>FFFF FF00		
8	>FFFF FEE0	NMI	Nonmaskable interrupt
9	>FFFF FEC0	HI	Host interrupt
10	>FFFF FEA0	DI	Display interrupt
11	>FFFF FE80	WV	Window violation
12	>FFFF [illegible]	Traps 12–29	
13	>FFFF [illegible]		
14	>FFFF [illegible]		
15	>FFFF [illegible]		
16	>FFFF [illegible]		
17	>FFFF [illegible]		
18	>FFFF [illegible]		
19	>FFFF [illegible]		
20	>FFFF [illegible]		
21	>FFFF [illegible]		
22	>FFFF [illegible]		
23	>FFFF [illegible]		
24	>FFFF [illegible]		
25	>FFFF [illegible]		
26	>FFFF [illegible]		
27	>FFFF [illegible]		
28	>FFFF [illegible]		
29	>FFFF [illegible]		
30	>FFFF FC20	ILLOP	Illegal opcode
31	>FFFF FC00	TRAP 31	

CONTROL Register

15	14–10	9	8	7–6	5	4–3	2	1–0
CD	PPOP	PBV	PBH	W	T	RR	RM	res

RM: DRAM Refresh Mode
- 0 - [illegible] only
- 1 - RAS-before-CAS

RR: DRAM Refresh Rate
- 00 - Every 32 LCLKs
- 01 - Every 64 LCLKs
- 10 - Reserved
- 11 - No DRAM refresh

T: 0 - Disable transparency; 1 - Enable transparency

W: Window detection
- 00 - No windowing
- 01 - Window hit
- 10 - Window miss
- 11 - Window clip

PBH: PixBlt Horizontal Direction
- 0 - Increment X
- 1 - Decrement X

PBV: PixBlt Vertical Direction
- 0 - Increment Y
- 1 - Decrement Y

PPOP: Pixel Processing Operation

CD: 0 - Enable cache; 1 - Disable cache

DPYCTL Register

15	14	13	12	11	10	9–2	1	0
ENV	NIL	DXV	SRE	SRT	ORG	DUDATE	res	HSD

HSD: Horizontal Sync Dir.

DUDATE:
- 00000000 - 0
- 00000001 - 1
- 00000010 - 2
- 00000100 - 4
- 00001000 - 8
- 00010000 - 16
- 00100000 - 32
- 01000000 - 64
- 10000000 - 128

ORG: Screen Origin Select
- 0 - Upper left corner
- 1 - Lower left corner

SRT: Shift-Register Transfer
- 0 - Normal pixel accesses
- 1 - VRAM-shift-reg. cycles

SRE: 0 - Disable screen refresh; 1 - Enable screen refresh

DXV: 0 - Disable external video; 1 - Enable external video

NIL: 0 - Interlaced video; 1 - Noninterlaced video

ENV: 0 - Blank entire screen; 1 - Enable video

HSTCTLH Register

15	14	13	12	11	10	9	8	7–0
HLT	CF	LBL	INCW	INCR	res	NMIM	NMI	reserved

NMI:NMIM:

NMI	NMIM	
0	0	No effect
0	1	Undefined
1	0	NMI (save context)
1	1	NMI (discard context)

INCR: 0 - No increment; 1 - Increment address before read

INCW: 0 - No increment; 1 - Increment address after write

LBL: Lower Byte Last
- 0 - Access MSBs of HSTDATA and HSTADRH 1st
- 1 - Access LSBs of HSTDATA and HSTADRL 1st

CF: 0 - No effect; 1 - Flush and disable cache

HLT: 0 - Allow GSP to run; 1 - Halt GSP instruction execution

HSTCTLL Register

15–8	7	6–4	3	2–0
reserved	INTOUT	MSGOUT	INTIN	MSGIN

MSGIN: Message in, host to GSP

INTIN: Interrupt in, host to GSP
- 0 - No interrupt request
- 1 - Send interrupt request to GSP

MSGOUT: Message out, GSP to host

INTOUT: Interrupt out, GSP to host
- 0 - No interrupt request
- 1 - Send interrupt request to host

INTENB Register

15–11	10	9	8	7–3	2	1	0
reserved	WVE	DIE	HIE	reserved	X2E	X1E	res

0 = Disabled, 1 = Enabled

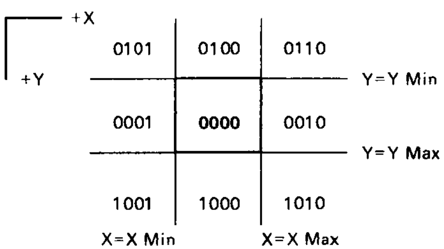
X1	External interrupt 1	**HI**	Host interrupt
X2	External interrupt 2	**DI**	Display interrupt
		WV	Window violation interrupt

INTPEND Register

15–11	10	9	8	7–3	2	1	0
reserved	WVP	DIP	HIP	reserved	X2P	X1P	res

0 = No interrupt request, 1 = Interrupt request pending

CPW Instruction (Outcodes)



Pixel Processing Operations

PPOP Field	Operation
00000	Source → Destination
00001	Source AND Destination → Destination
00010	Source AND ~Destination → Destination
00011	0s → Destination
00100	Source OR ~Destination → Destination
00101	Source XNOR Destination → Destination
00110	~Destination → Destination
00111	Source NOR Destination → Destination
01000	Source OR Destination → Destination
01001	Destination → Destination
01010	Source XOR Destination → Destination
01011	~Source AND Destination → Destination
01100	1s → Destination
01101	~Source OR Destination → Destination
01110	Source NAND Destination → Destination
01111	~Source → Destination
10000	Source + Destination → Destination
10001	ADDS(Source, Destination) → Destination
10010	Destination - Source → Destination
10011	SUBS(Source, Destination) → Destination
10100	MAX(Source, Destination) → Destination
10101	MIN(Source, Destination) → Destination
10110–11111	Reserved

TMS34010 Instruction Set

Syntax	Words	Mach. States	16-Bit Opcode MSB … LSB
ABS Rd	1	1,4	[illegible]
[illegible]	1	1,4	[illegible]
[illegible]	1	1,4	[illegible]
[illegible]	2	2,8	[illegible]
[illegible]	3	3,12	[illegible]
[illegible] K,Rd	1	1,4	[illegible]
[illegible] Rd	1	[illegible]	[illegible]
[illegible] Rd	3	[illegible]	[illegible]
[illegible] Rd	1	[illegible]	[illegible]
[illegible] L,Rd	3	[illegible]	[illegible]
[illegible] Rs,Rd	1	[illegible]	[illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible] Rs,Rd	1	2,5	[illegible]
CALL Rs	1	3+(3),9 3+(9),15	0000 1001 [illegible]
CALLA Addr	3	4+(2),15 4+(8),21	0000 1101 0101 1111
CALLR Addr	2	3+(2),11 3+(8),17	0000 1101 0011 1111
CLR Rd	1	1,4	[illegible] 011D [illegible]
[illegible]	1	1,4	[illegible] 0011 [illegible]
[illegible]	1	1,4	[illegible] 1011 [illegible]
[illegible]	2	2,8	[illegible] 1011 [illegible]
[illegible] L,Rd	3	3,12	[illegible]
[illegible] XY Rd,Rd	1	3,6	[illegible]
[illegible] Rs,Rd	1	1,4	1110 [illegible]
[illegible] L Rs,Rd	1	3,6	1110 [illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible]	1	3,6	[illegible] 0011 [illegible]
[illegible] Rs,Rd	1	40,43 39,42	[illegible] 100S SSSR [illegible]
[illegible] Rs Rd	1	37,40	[illegible] 101S [illegible] DDDD
[illegible] Rs,Rd	1	†	[illegible] 011S [illegible]
DSJ Rd,Addr	2	3,9 2,8	0000 1101 [illegible]
DSJEQ Rd,Addr	2	3,9 2,8	0000 1101 101R DDDD
DSJNE Rd,Addr	2	3,9 2,8	0000 1101 110R DDDD
DSJS Rd,Addr	1	2,5 3,6	0011 1DKK KKKR DDDD
[illegible]	1	3,6	[illegible] 1101 0110 [illegible]
[illegible]	1	6,9	[illegible]
[illegible] Rd,F	1	1,4	[illegible]
[illegible] Rd	1	2,5	[illegible]
[illegible] L	1	†	[illegible]
FILL XY	1	†	[illegible] 1110 [illegible]
[illegible] Rd	1	1,4	[illegible] 010R [illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible] Addr	3	3,6 4,7	[illegible]
JRcc Addr	2	3,6 1,4	1100 code 0000 0000
JRcc Addr	1	2,5 2,5	1100 code xxxx xxxx
[illegible] MP Rs	1	2,5	[illegible] 011R [illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible]	1	†	[illegible]
[illegible] Rs,*Rd	1	†	[illegible]
[illegible] *Rs,Rd	1	†	[illegible]
[illegible] *Rs,*Rd	1	†	[illegible]
[illegible] *Rs,*R[illegible])	2	†	1010 [illegible]
[illegible] *Rs(Disp),Rd	2	†	1010 [illegible]
MOVB *Rs(Disp), *F[illegible]	3	†	1011 110S [illegible]

† See TMS34010 User's Guide

TMS34010 Instruction Set (Continued)

Syntax	Words	Mach. States	16-Bit Opcode MSB … LSB
MOVB R[illegible] Addr	3	†	[illegible] 0101 111R [illegible]
[illegible] Addr,Rd	3	†	[illegible] 0111 111R [illegible]
[illegible] Addr, [illegible] Addr	5	†	[illegible] 0011 0100 [illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible] Rs,*Rd,F	1	†	[illegible]
[illegible] Rs,-*Rd,F	1	†	[illegible] 00FS [illegible]
[illegible] Rs,*Rd+,F	1	†	[illegible] 00FS [illegible]
[illegible] *Rs,Rd,F	1	†	[illegible] 01FS [illegible]
MOVE -*Rs,Rd,F	1	†	[illegible] 01FS [illegible]
MOVE *Rs+,Rd,F	1	†	[illegible] 01FS [illegible]
MOVE *Rs,*Rd,F	1	†	[illegible] 10FS [illegible]
[illegible] -*Rs,-*Rd,F	1	†	[illegible] 10FS [illegible]
[illegible] *Rs+,*Rd+,F	1	†	[illegible] 10FS [illegible]
[illegible] Rs,[illegible]),F	2	†	1011 00FS [illegible]
[illegible] *Rs(Disp),Rd,F	2	†	1011 [illegible]
[illegible] *Rs(Disp), *Rd+,F	2	†	1101 [illegible]
MOVE *Rs(Disp), [illegible]	3	†	1011 10FS SSSR DDDD
[illegible] Addr,F	3	†	[illegible] 01F1 [illegible]
[illegible] Addr,Rd,F	3	†	[illegible] 01F1 [illegible]
[illegible] Addr,*Rd+,F	3	†	[illegible] 01F0 [illegible]
[illegible] Addr, [illegible] Addr,F	5	†	0000 01F1 [illegible]
[illegible] Rs,Rd	1	1,4	1110 110S [illegible]
[illegible] Rs,Rd	1	1,4	1110 111S [illegible]
[illegible] Rs,List	2	†	[illegible]
[illegible] Rs,List	2	†	[illegible]
[illegible] Rs,Rd	1	40,43	[illegible]
[illegible] Rs,Rd	1	35,38	[illegible] 111S [illegible]
[illegible] W,Rd	2	2,8	[illegible]
[illegible] L,Rd	3	3,12	[illegible]
MOVK K,Rd	1	1,4	[illegible]
MPYS Rs,Rd	1	20,23	[illegible]
MPYU Rs,Rd	1	21,24	[illegible] 111S [illegible]
[illegible]	1	1,4	[illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible]	1	1,4	[illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible] Rd	3	3,12	[illegible]
[illegible] B,L	1	†	[illegible] 1111 [illegible]
[illegible] B,XY	1	†	[illegible] 1111 [illegible]
[illegible] L,L	1	†	[illegible] 1111 [illegible]
[illegible]	1	†	[illegible] 1111 [illegible]
[illegible]	1	†	[illegible] 1111 [illegible]
[illegible] XY,XY	1	†	[illegible]
PIXT Rs,*Rd	1	†	[illegible]
PIXT Rs,*Rd.XY	1	†	1111 [illegible]
PIXT *Rs,Rd	1	†	1111 [illegible]
PIXT *Rs,*Rd	1	†	1111 [illegible]
PIXT *Rs.XY,Rd	1	†	1111 [illegible]
PIXT *Rs.XY,*Rd.XY	1	†	1111 [illegible]
POPST	1	8,11 10,13	0000 [illegible]
PUSHST	1	2+(3),8 2+(8),13	0000 0001 1110 0000
[illegible] Rs	1	3,6	[illegible]
RETI	1	11,14 [illegible]	[illegible]
RETS [N]	1	[illegible] 9,12	0000 1001 011N NNNN

† See TMS34010 User's Guide

TMS34010 Instruction Set (Concluded)

Syntax	Words	Mach. States	16-Bit Opcode MSB … LSB
RL K,Rd	1	1,4	[illegible]
RL Rs,Rd	1	1,4	[illegible]
[illegible]	1	1,4	[illegible]
[illegible] S,FE,F	1	1,4 2,5	[illegible] 01F1 01FS [illegible]
SEXT Rd,F	1	3,6	[illegible]
SLA K,Rd	1	3,6	[illegible]
SLA Rs,Rd	1	3,6	[illegible]
SLL K,Rd	1	1,4	[illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible] K,Rd	1	1,4	[illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible] K,Rd	1	1,4	[illegible] 11KK [illegible]
[illegible] Rs,Rd	1	1,4	[illegible] 011S [illegible]
[illegible]	1	1,4	[illegible] 010S [illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible]	2	2,8	[illegible]
[illegible]	3	3,12	[illegible] 111R [illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible]	1	1,4	[illegible]
[illegible] Rs,Rd	1	1,4	1110 [illegible]
[illegible]	1	[illegible]	0000 [illegible]
[illegible]	3	[illegible]	[illegible]
[illegible]	1	1,4	[illegible]

† See TMS34010 User's Guide

TMS34010 Directives

Directive and Syntax		Description
.align	†	Align SPC on 32-w[illegible] boundary
.bss <name>,<expr1>, <expr2>		[illegible] ible into .bss (uninitialized [illegible] on
.byte <expr>,,,	†	[illegible] successive bytes in current [illegible]
.copy <filename>	†	[illegible] urce file
.data	†	[illegible] nto .data (initialized data) section
.dim <expr>,,,		Sp[illegible] array dimensions for symbol
.end	†	Program end
.endef		[illegible] symbol [illegible]
.even	†	[illegible] SPC on [illegible] undary
.field <expr1>[,<expr2>]	†	[illegible] ield
.file <string>		[illegible]
[illegible]		[illegible]
.globl [illegible]	†	[illegible]
.int [illegible]		[illegible] integer
.long [illegible]>,,,	†	[illegible] 32-bit field
.line [illegible]>[,<expr2>]		[illegible] number for definition
.list	†	[illegible] source [illegible]
.ln <expr>,,,		[illegible] r record
.mlib <pathname>'	†	[illegible]
.nolist	†	[illegible]
.option <option list>	†	[illegible]
.page		[illegible] e listing
.scl [illegible]		[illegible] for [illegible] ition
.sect [illegible]>'	†	[illegible] user- [illegible] d section
<sym> .set <expr>		[illegible]
.size [illegible]>		[illegible] definition
.space <expr>	†	Reserve <expr> amount of space in [illegible]
.string [-]'<string>'	†	Initialize text
.tag <name>		Set tag field for d[illegible] on
.text	†	Assemble into [illegible] (executable [illegible] section
.title '<string>'	†	[illegible] source page heading
.type [illegible]>		[illegible] tion
.val <[illegible]		[illegible] definition
.word <expr>,,,	†	[illegible] word

† These directives may use a label, if desired)

Symbols and Abbreviations

Symbol	Description	Symbol	Description
Rs	Source register	Rd	Destination register
Rs.X	X [illegible] of Rs	Rd.X	X half of Rd
Rs.Y	Y [illegible] of Rs	Rd.Y	Y half of Rd
[illegible]	[illegible] ssion	[illegible]	[illegible]
[illegible]	[illegible] te address	[illegible]	[illegible] on address
[illegible]	[illegible] mmediate value	[illegible]	[illegible] te value
K	[illegible] constant	Disp	Displa[illegible]
*	Indirect ad[illegible]	@	[illegible] ng
[ ]	Opt[illegible]	{ }	[illegible]
< >	Sub[illegible] value or register for the text in the brackets.		

ASCII Character Set

	0–	1–	2–	3–	4–	5–	6–	7–
–0	[illegible]	[illegible]	SP	0	@	P	'	p
–1	[illegible]	[illegible]	!	1	A	Q	a	q
–2	[illegible]	[illegible]	"	2	B	R	b	r
–3	[illegible]	[illegible]	#	3	C	S	c	s
–4	[illegible]	[illegible]	$	4	D	T	d	t
–5	[illegible]	[illegible]	%	5	E	U	e	u
–6	[illegible]	[illegible]	&	6	F	V	f	v
–7	[illegible]	ETB	'	7	G	W	g	w
–8	[illegible]	[illegible]	(	8	H	X	h	x
–9	HT	[illegible]	)	9	I	Y	i	y
–A	LF	[illegible]	*	:	J	Z	j	z
–B	VT	[illegible]	+	;	K	[	k	{
–C	FF	[illegible]	,	<	L	\	l	|
–D	CR	GS	–	=	M	]	m	}
–E	SO	RS	.	>	N	^	n	~
–F	SI	US	/	?	O	_	o	DEL

RTC Training Numbers

For assistance in using TMS340 products, call the TI Regional Technology Center (RTC) nearest you.

USA:

Atlanta	(404) 662-7945
Boston	(617) 895-9196
Chicago	(312) 640-[illegible]
Dallas	(214) 680-[illegible]
Northern California	(408) 748-[illegible]
Southern California	(714) 660-8[illegible]

Canada:

Nepean, Ontario	(613) 726-1970

Graphics Hotline Number

(713) TRY-A340

TEXAS INSTRUMENTS

TMS34010 Programmer's Reference

Memory Map

Address	15 — 0	
>FFFF FFF0 >FFFF FC00	64 words	Interrupt vectors
>FFFF FBF0 >FFFF E000	512 words	Reserved
>FFFF DFF0 >C000 2000	2^{26} - 1024 words	General use
>C000 1FF0 >C000 0200	512 words	Reserved
>C000 01F0 >C000 0000	32 words	I/O registers
>BFFF FFF0 >0000 0000	3×2^{26} words	General use

Status Register

31	30	29	28	27	26	25–22	21	20–12	11	10–6	5	4–0
N	C	Z	V	res	PBX	res	IE	reserved	FE1	FS1	FE0	FS0

- **N** Sign bit (or X=0)
- **C** Carry bit (or Y<0)
- **Z** Zero bit (or Y=0)
- **V** Overflow bit (or X<0)
- **PBX** PixBlt executing bit
- **IE** Interrupt enable
- **FE1** Field extension bit 1
- **FS1** Field size bit 1
- **FE0** Field extension bit 0
- **FS0** Field size bit 0

Register File B

	31(MSB) — 0(LSB)	
B0	[illegible]DR	Source Address
B1	[illegible]H	Source Pitch
B2	[illegible]	Destination Address
B3	[illegible]	Destination Pitch
B4	[illegible]	Offset
B5	[illegible]	Window Start
B6	[illegible]	Window End
B7	[illegible]	Delta Y/Delta X
B8	[illegible]	Color 0
B9	[illegible]	Color 1
B10	Temporary Register	
B11	Temporary Register	Used as temporary storage for PIXBLTs and FILLS
B12	Temporary Register	
B13	Temporary Register	
B14	Temporary Register	
SP	Stack Pointer	

I/O Registers

Address	15 — 0	
>C000 01F0	[illegible]	DRAM refresh count
>C000 01E0	[illegible]	Display address
>C000 01D0	[illegible]	Vertical count
>C000 01C0	[illegible]	Horizontal count
>C000 01B0	[illegible]	Display tap point
>[illegible]01A0 >[illegible]0170	Reserved	
>C000 0160	[illegible]	Plane mask
>C000 0150	[illegible]	Pixel size
>C000 0140	[illegible]	Conversion (dest. pitch)
>C000 0130	[illegible]	Conversion (source pitch)
>C000 0120	[illegible]	Interrupt pending
>C000 0110	[illegible]	Interrupt enable
>C000 0100	[illegible]	Host control, 8 MSBs
>C000 00F0	[illegible]	Host control, 8 LSBs
>C000 00D0	[illegible]	Host address, 16 MSBs
>C000 00E0	[illegible]	Host address, 16 LSBs
>C000 00C0	[illegible]	Host data
>C000 00B0	[illegible]	I/O control
>C000 00A0	[illegible]	Display interrupt
>C000 0090	[illegible]	Display start
>C000 0080	[illegible]	Display control
>C000 0070	[illegible]	Vertical total
>C000 0060	[illegible]	Vertical start blank
>C000 0050	[illegible]	Vertical end blank
>C000 0040	[illegible]	Vertical end sync
>C000 0030	[illegible]	Horizontal total
>C000 0020	[illegible]	Horizontal start blank
>C000 0010	[illegible]NK	Horizontal end blank
>C000 0000	[illegible]NC	Horizontal end sync

Vector Address Map

Trap Number	Address	32 — 0	
0	>FFFF FFE0	[illegible]	Reset
1	>FFFF FFC0	[illegible]	External interrupt 1
2	>FFFF FFA0	INT2	External interrupt 2
3	>FFFF FF80	Traps 3–7	
4	>FFFF FF60		
5	>FFFF FF40		
6	>FFFF FF20		
7	>FFFF FF00		
8	>FFFF FEE0	[illegible]	Nonmaskable interrupt
9	>FFFF FEC0	[illegible]	Host interrupt
10	>FFFF FEA0	DI	Display interrupt
11	>FFFF FE80	WV	Window violation
12	>FFFF [illegible]	Traps 12–29	
13	>FFFF [illegible]		
14	>FFFF [illegible]		
15	>FFFF [illegible]		
16	>FFFF [illegible]		
17	>FFFF [illegible]		
18	>FFFF [illegible]		
19	>FFFF [illegible]		
20	>FFFF [illegible]		
21	>FFFF [illegible]		
22	>FFFF [illegible]		
23	>FFFF [illegible]		
24	>FFFF [illegible]		
25	>FFFF [illegible]		
26	>FFFF [illegible]		
27	>FFFF [illegible]		
28	>FFFF FC60		
29	>FFFF FC40		
30	>FFFF FC20	[illegible]	Illegal opcode
31	>FFFF FC00	[illegible]	

CONTROL Register

15	14–10	9	8	7–6	5	4–3	2	1–0
CD	PPOP	PBV	PBH	W	T	RR	RM	res

RM: DRAM Refresh Mode
- 0 - [illegible] only
- 1 - [illegible] before-CAS

RR: DRAM Refresh Rate
- 00 - Every 32 LCLKs
- 01 - Every 64 LCLKs
- 10 - Reserved
- 11 - No DRAM refresh

T:
- 0 - Disable transparency
- 1 - Enable transparency

W: Window detection
- 00 - No windowing
- 01 - Window hit
- 10 - Window miss
- 11 - Window clip

PBH: PixBlt Horizontal Direction
- 0- Increment X
- 1 - Decrement X

PBV: PixBlt Vertical Direction
- 0 - Increment Y
- 1 - Decrement Y

PPOP: Pixel Processing Operation

CD:
- 0 - Enable cache
- 1 - Disable cache

DPYCTL Register

15	14	13	12	11	10	9–2	1	0
ENV	NIL	DXV	SRE	SRT	DRG	DUDATE	res	HSD

HSD: Horizontal Sync Dir.

DUDATE:
- 00000000 - 0
- 00000001 - 1
- 00000010 - 2
- 00000100 - 4
- 00001000 - 8
- 00010000 - 16
- 00100000 - 32
- 01000000 - 64
- 10000000 - 128

DRG: Screen Origin Select
- 0 - Upper left corner
- 1 - Lower left corner

SRT: Shift-Register Transfer
- 0 - Normal pixel accesses
- 1 - VRAM-shift-reg. cycles

SRE:
- 0 - Disable screen refresh
- 1 - Enable screen refresh

OXV:
- 0 - Disable external video
- 1 - Enable external video

NIL:
- 0 - Interlaced video
- 1 - Noninterlaced video

ENV:
- 0 - Blank entire screen
- 1 - Enable video

HSTCTLH Register

15	14	13	12	11	10	9	8	7–0
HLT	CF	LBL	INCW	INCR	res	NMIM	NMI	reserved

NMI:NMIM:

NMI	NMIM	
0	0	No effect
0	1	Undefined
1	0	NMI (save context)
1	1	NMI (discard context)

INCR:
- 0 - No increment
- 1 - Increment address before read

INCW:
- 0 - No increment
- 1 - Increment address after write

LBL: Lower Byte Last
- 0 - Access MSBs of HST-DATA and HSTADRH 1st
- 1 - Access LSBs of HST-DATA and HSTADRL 1st

CF:
- 0 - No effect
- 1 - Flush and disable cache

HLT:
- 0 - Allow GSP to run
- 1 - Halt GSP instruction execution

HSTCTLL Register

15–8	7	6–4	3	2–0
reserved	INTOUT	MSGOUT	INTIN	MSGIN

MSGIN: Message in, host to GSP

INTIN: Interrupt in, host to GSP
- 0 - No interrupt request
- 1 - Send interrupt request to GSP

MSGOUT: Message out, GSP to host

INTOUT: Interrupt out, GSP to host
- 0 - No interrupt request
- 1 - Send interrupt request to host

INTENB Register

15–11	10	9	8	7–3	2	1	0
reserved	WVE	DIE	HIE	reserved	X2E	X1E	res

0 = Disabled, 1 = Enabled

- **X1** External interrupt 1
- **X2** External interrupt 2
- **HI** Host interrupt
- **DI** Display interrupt
- **WV** Window violation interrupt

INTPEND Register

15–11	10	9	8	7–3	2	1	0
reserved	WVP	DIP	HIP	reserved	X2P	X1P	res

0 = No interrupt request, 1 = Interrupt request pending

CPW Instruction (Outcodes)

(+X to the right, +Y downward)

	X<X Min	X Min ≤ X ≤ X Max	X>X Max
above Y=Y Min	0101	0100	0110
between Y=Y Min and Y=Y Max	0001	0000	0010
below Y=Y Max	1001	1000	1010

Boundaries: Y=Y Min, Y=Y Max, X=X Min, X=X Max

Pixel Processing Operations

PPOP Field	Operation
00000	Source → Destination
00001	Source AND Destination → Destination
00010	Source AND ~Destination → Destination
00011	0s → Destination
00100	Source DR ~Destination → Destination
00101	Source XNDR Destination → Destination
00110	~Destination → Destination
00111	Source NDR Destination → Destination
01000	Source DR Destination → Destination
01001	Destination → Destination
01010	Source XDR Destination → Destination
01011	~Source AND Destination → Destination
01100	1s → Destination
01101	~Source DR Destination → Destination
01110	Source NAND Destination → Destination
01111	~Source → Destination
10000	Source + Destination → Destination
10001	ADDS(Source, Destination) → Destination
10010	Destination - Source → Destination
10011	SUBS(Source, Destination) → Destination
10100	MAX(Source, Destination) → Destination
10101	MIN(Source, Destination) → Destination
10110–11111	Reserved

TMS34010 Instruction Set

Syntax	Words	Mach. States	16-Bit Opcode MSB … LSB
[illegible]d	1	1,4	[illegible]
[illegible]	1	1,4	[illegible]
[illegible]	1	1,4	[illegible]
[illegible]	2	2,8	1011 [illegible]
[illegible]	3	3,12	[illegible]
[illegible]K,Rd	1	1,4	[illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible] Rd	3	3,12	[illegible]
[illegible] Rd	1	1,4	[illegible] DI[illegible]
[illegible],Rd	3	3,12	[illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible],Rd	1	1,4	[illegible]
BTST Rs,Rd	1	2,5	[illegible]
CALL Rs	1	3+(3),9 3+(9),15	[illegible]
CALLA Addr	3	4+(2),15 4+(8),21	0000 1101 0101 1111
CALLR Addr	2	3+(2),11 3+(8),17	0000 1101 0011 1111
CLR Rd	1	1,4	0101 011D [illegible]
[illegible]	1	1,4	[illegible]0011 [illegible]
[illegible]	1	1,4	[illegible]1011 [illegible]
[illegible]	2	2,8	[illegible]1011 [illegible]
[illegible]	3	3,12	[illegible] 011R
[illegible]XY Rd,Rd	1	3,6	[illegible]
[illegible],Rd	1	1,4	1110 [illegible]
[illegible] Rs,Rd	1	3,6	1110 [illegible]
[illegible]	1	1,4	[illegible]
[illegible]	1	3,6	[illegible] 0110 [illegible]
[illegible] Rs,Rd	1	40,43 39,42	[illegible] SSSR [illegible]
DIVU Rs,Rd	1	37,40	0101 [illegible]
DRAV Rs,Rd	1	†	1111 [illegible]
DSJ Rd,Addr	2	3,9 2,8	0000 1101 [illegible]
DSJEQ Rd,Addr	2	3,9 2,8	0000 1101 101R DDDD
DSJNE Rd,Addr	2	3,9 2,8	0000 1101 110R DDDD
DSJS Rd,Addr	1	2,5 3,6	0011 1DKK KKKR DDDD
[illegible]	1	3,6	[illegible] 0000
[illegible]	1	6,9	[illegible]
[illegible] Rd,F	1	1,4	[illegible]
[illegible]C Rd	1	2,5	[illegible]
[illegible]	1	†	[illegible]
FILL XY	1	†	1111 1110
[illegible] Rd	1	1,4	[illegible] D [illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible] Addr	3	3,6 4,7	[illegible] code [illegible]
JRcc Addr	2	3,6 1,4	1100 code 0000 0000
JRcc Addr	1	2,5 2,5	1100 code xxxx xxxx
[illegible] Rs	1	2,5	[illegible] 011R [illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible]	1	†	[illegible]
[illegible] Rs,*Rd	1	†	[illegible] 110S [illegible]
MOVB *Rs,Rd	1	†	[illegible] 111S [illegible]
MOVB *Rs,*Rd	1	†	[illegible] 110S [illegible]
[illegible]B *Rs,*R[illegible]	2	†	1010 [illegible]
[illegible] *Rs(Disp),Rd	2	†	1010 [illegible]
[illegible] *Rs(Disp), *R[illegible]	3	†	1011 110S [illegible]

† See [illegible]010 User's Guide

TMS34010 Instruction Set (Continued)

Syntax	Words	Mach. States	16-Bit Opcode MSB … LSB
[illegible]Addr	3	†	[illegible] 0101 111R [illegible]
[illegible]Addr,Rd	3	†	[illegible] 0111 111R [illegible]
[illegible]Addr, [illegible]Addr	5	†	0000 0011 0100 0000
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible] Rs	1	†	[illegible]
[illegible] Rs,-*Rd,F	1	†	[illegible] 00FS [illegible]
[illegible] Rs,*Rd+,F	1	†	[illegible] 00FS [illegible]
[illegible] Rd,F	1	†	[illegible] 01FS [illegible]
[illegible] *Rs,Rd,F	1	†	[illegible] 01FS [illegible]
[illegible] *Rs-[illegible]	1	†	[illegible] 01FS [illegible]
[illegible] *Rs,[illegible]	1	†	[illegible] 10FS [illegible]
[illegible] *Rs,-*Rd,F	1	†	[illegible] 10FS [illegible]
[illegible] *Rs+,*Rd+,F	1	†	1001 10FS [illegible]
[illegible] Rs[illegible]),F	2	†	[illegible] 00FS [illegible]
[illegible] *Rs(Disp),Rd,F	2	†	1011 01FS [illegible]
[illegible] *Rs(Disp), *Rd+,F	2	†	1101 00FS [illegible]
MOVE [illegible]Disp), *R[illegible]	3	†	1011 10FS SSSR DDDD
[illegible]E [illegible]ddr,F	3	†	[illegible] 01F1 [illegible]
[illegible]F @SAddr,Rd,F	3	†	[illegible] 01F1 [illegible]
[illegible]dr,*Rd+,F	3	†	[illegible] 01F0 [illegible]
[illegible]dr, [illegible]Addr,F	5	†	0000 01F1 1100 DD[illegible]
[illegible] Rs,Rd	1	1,4	1110 [illegible]
[illegible] Rs Rd	1	1,4	1110 [illegible]
[illegible] Rs,List	2	†	[illegible] 1001 [illegible]
[illegible] Rs,List	2	†	[illegible]
[illegible] Rs,Rd	1	40,43	[illegible]
[illegible] Rs Rd	1	35,38	[illegible]
[illegible]	2	2,8	[illegible]
[illegible],Rd	3	3,12	[illegible]
[illegible] K,Rd	1	1,4	[illegible]
[illegible] Rs,Rd	1	20,23	[illegible]
MPYU Rs,Rd	1	21,24	[illegible] 111S [illegible]
[illegible]	1	1,4	[illegible] 0011 [illegible]
[illegible]d	1	1,4	[illegible] 0011 [illegible]
[illegible]	1	1,4	[illegible] 0011 [illegible]
[illegible] Rd	1	1,4	[illegible] 0011 [illegible]
[illegible]s,Rd	1	1,4	[illegible] 010S [illegible]
[illegible] Rd	3	3,12	[illegible] 1011 [illegible]
[illegible] B,L	1	†	1111 [illegible]
[illegible] B,XY	1	†	1111 [illegible]
[illegible] L,L	1	†	1111 0000
[illegible] L,XY	1	†	1111 [illegible]
[illegible] XY,L	1	†	1111 [illegible]
[illegible] XY,XY	1	†	[illegible]
[illegible] Rs,*Rd	1	†	[illegible]
PIXT Rs,*Rd.XY	1	†	1111 [illegible]
PIXT *Rs,Rd	1	†	1111 [illegible]
PIXT *Rs,*Rd	1	†	1111 [illegible]
PIXT *Rs.XY,Rd	1	†	1111 [illegible]
PIXT *Rs.XY,*Rd.XY	1	†	1111 [illegible]
POPST	1	8,11	0000 0001 [illegible]
PUSHST	1	2+(3),8 2+(8),13	0000 0001 1110 0000
[illegible] Rs	1	3,6	[illegible] 0001 101R [illegible]
RETI	1	11,14 15,18	[illegible] 1001 0100 [illegible]
RETS [N]	1	7,10 9,12	0000 1001 011N NNNN

† See TMS34010 User's Guide

TMS34010 Instruction Set (Concluded)

Syntax	Words	Mach. States	16-Bit Opcode MSB … LSB
RL K,Rd	1	1,4	[illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
[illegible]	1	1,4	[illegible]
[illegible] FS,FE,F	1	1,4 2,5	[illegible] 01F1 01FS [illegible]
SEXT Rd,F	1	3,6	[illegible]
SLA K,Rd	1	3,6	[illegible]
SLA Rs,Rd	1	3,6	[illegible]
SLL K,Rd	1	1,4	0010 [illegible]KK [illegible]
[illegible] Rs,Rd	1	1,4	0110 [illegible]
[illegible] K,Rd	1	1,4	0010 [illegible]
[illegible] Rs,Rd	1	1,4	0110 [illegible]
[illegible] K,Rd	1	1,4	0010 11KK [illegible]
[illegible] Rs,Rd	1	1,4	0110 011S [illegible]
[illegible] Rs,Rd	1	1,4	[illegible] 010S [illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible]	2	2,8	[illegible]
[illegible] Rd	3	3,12	[illegible]
[illegible] K,Rd	1	1,4	[illegible]
[illegible] Rd	1	1,4	[illegible]
[illegible] Rs,Rd	1	1,4	[illegible]
TRAP [illegible]	1	16,19	0000 [illegible]
[illegible]	3	[illegible]	1011 110D [illegible]
[illegible]	1	1,4	[illegible] 01F1 001R

† See TMS34010 User's Guide

TMS34010 Directives

Directive and Syntax		Description
.align	†	Align SPC on 32-word boundary
.bss <name>,<expr1>, <expr2>		Assemble into .bss (uninitialized data) section
.byte <expr>,..	†	Initialize successive bytes in current section
.copy <filename>	†	Include source file
.data	†	Assemble into .data (initialized data) section
.dim <expr>,..		Specify array dimensions for symbol
.end	†	Program end
.endef		End a symbol definition
.even	†	Align SPC on word boundary
.field <expr1>[,<expr2>]	†	Initialize variable-length field
.file <string>		Define program identifier
.file <filename>		Define current file
.globl <symbol>,..	†	External definition
.int <expr>,..		Initialize 32-bit integer
.long <expr>,..	†	Initialize 32-bit field
.line <expr1>[,<expr2>]		Set line number for definition
.list	†	Restart source listing
.ln <expr>,..		Generate a line number record
.mlib '<pathname>'	†	Define macro library
.nolist	†	Stop source listing
.option <option list>	†	Output options
.page	†	Page eject source listing
.scl <expr>		Set storage class for definition
.sect '<name>'	†	Assemble into user-defined section
<symbol> .set <expr>		Initialize symbol
.size <expr>		Set size field for definition
.space <expr>	†	Reserve <expr> amount of space in current section
.string [-]'<string>'	†	Initialize text
.tag <name>		Set tag field for definition
.text	†	Assemble into .text (executable code) section
.title '<string>'	†	Print title in source page heading
.type <expr>		Set type field for definition
.val <expr>		Set value for definition
.word <expr>,..	†	Initialize word

† These directives may use a label (if desired)

Symbols and Abbreviations

Symbol	Description	Symbol	Description
Rs	S[illegible]	Rd	[illegible]tion register
Rs.X	X [illegible]	Rd.X	X [illegible] of Rd
[illegible]	Y [illegible] of Rs	Rd.Y	Y [illegible] of Rd
[illegible]	Expression	addr	A[illegible]s
SAddr	Source address	DAddr	D[illegible]s
IW	16-bit [illegible]iate value	IL	32-bit [illegible] value
K	5-bit [illegible]t	Disp	[illegible]
*	In[illegible]addressing	@	[illegible]ssing
[ ]	O[illegible] para[illegible]	{ }	[illegible]
< >	Substitute a[illegible]r register for the [illegible]n the brackets.		

ASCII Character Set

	0–	1–	2–	3–	4–	5–	6–	7–
–0	[illegible]		SP	0	@	P	'	p
–1			!	1	A	Q	a	q
–2			"	2	B	R	b	r
–3			#	3	C	S	c	s
–4			$	4	D	T	d	t
–5			%	5	E	U	e	u
–6			&	6	F	V	f	v
–7		ETB	'	7	G	W	g	w
–8	BS		(	8	H	X	h	x
–9	HT		)	9	I	Y	i	y
–A	LF		*		J	Z	j	z
–B	VT		+	;	K	[	k	{
–C	FF		,	<	L	\	l	|
–D	CR	GS	–	=	M	]	m	}
–E	SO	RS	.	>	N	^	n	~
–F	SI	US	/	?	O	_	o	DEL

RTC Training Numbers

For assistance in using TMS340 products, call the TI Regional Technology Center (RTC) nearest you.

USA:

- Atlanta .... (404) 662-7945
- Boston .... (617) 895-9196
- Chicago .... (312) 640-2909
- Dallas .... (214) 680-5066
- Northern California .... (408) 748-2220
- Southern California .... (714) 660-8140

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